demmel products gmbh

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SPECIFICATION

DCD-MX70

For Customer's Acceptance:

Approved By	Comment

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT

2. Revision Record

Date	Rev.No.	Page	Revision Items	Prepared
2021.03.13	A		Thefirstrelease	

3. General Specifications

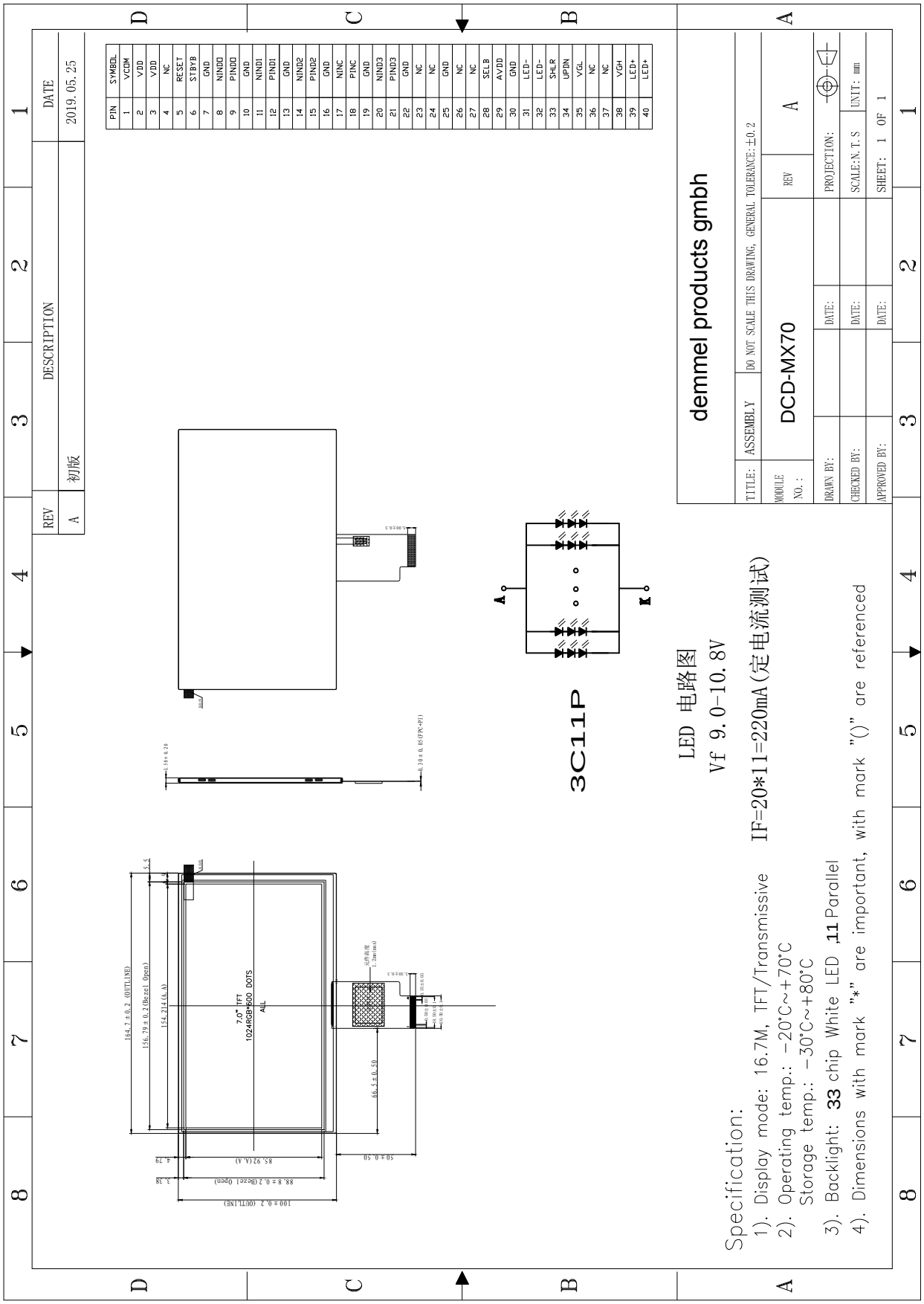
DCD-MX70 is a TFT-LCDmodule.It is composed of a TFT-LCDpanel, driver IC, FPC, a back light unit. The 7.0′′ display area contains1024 x 600 pixels and can display up to 16.7M colors. This productaccords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	Normally Black,Transmissive	-	
Display color	16.7M		1
Viewing Direction	ALL	O'Clock	
Operating temperature	-20~+70	℃	
Storage temperature	-30~+80	℃	
Module size	165.00(W)×100.00(H)×3.50(T)	mm	2
Active Area(W×H)	154.2144(W)×85.92(H)	mm	
Number of Dots	1024×RGB×600	dots	
Backlight	33-LEDs(white)	pcs	
Interface	LVDS Interface	-	
DriverIC	HX8282-A+HX8696-A		

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

4.Outline.Drawing



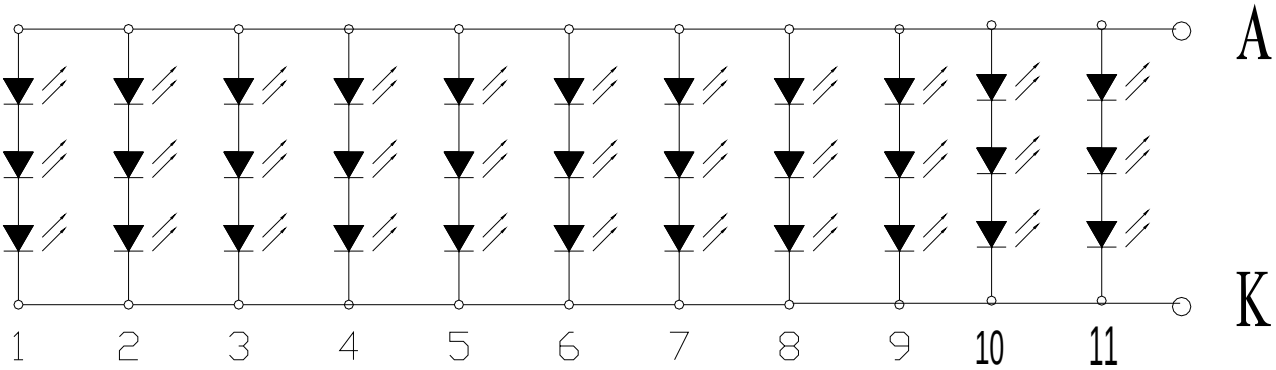
5.ElectricalSpecificationsandTimingCharacteristics

5.1Electricalcharacteristics(V ss=0V ,Ta=25℃)

Item	Symbol	Min.	Typ	Max.	Unit
Digital Supply Voltage	**VDD**	3.0	3.3	3.6	**V**
Analog Supply Voltage	**AVDD**	8.9	9.0	9.1	**V**
TFT Gate ON Voltage	**VGH**	17.0	18.0	19.0	**V**
TFT Gate OFF Voltage	**VGL**	-6.5	-6.0	-5.5	**V**
TFT Common Electrode Voltage	**VCOM**	3.0	3.15	3.3	**V**

5.2LEDbacklightspecification(V ss=0V ,Ta=25℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	-	-	9.0	9.6	10.8	V	1
Supply current	I_f	-	-	220	-	mA	2
LED Life Time	H_r	-	-	50000	-	Hr	



Note:

1: $V_{LED}=V_{LED}(+)-V_{LED}(-)$.

2:The current of LED is 20mA.

A LED drive in constant current mode is recommended.

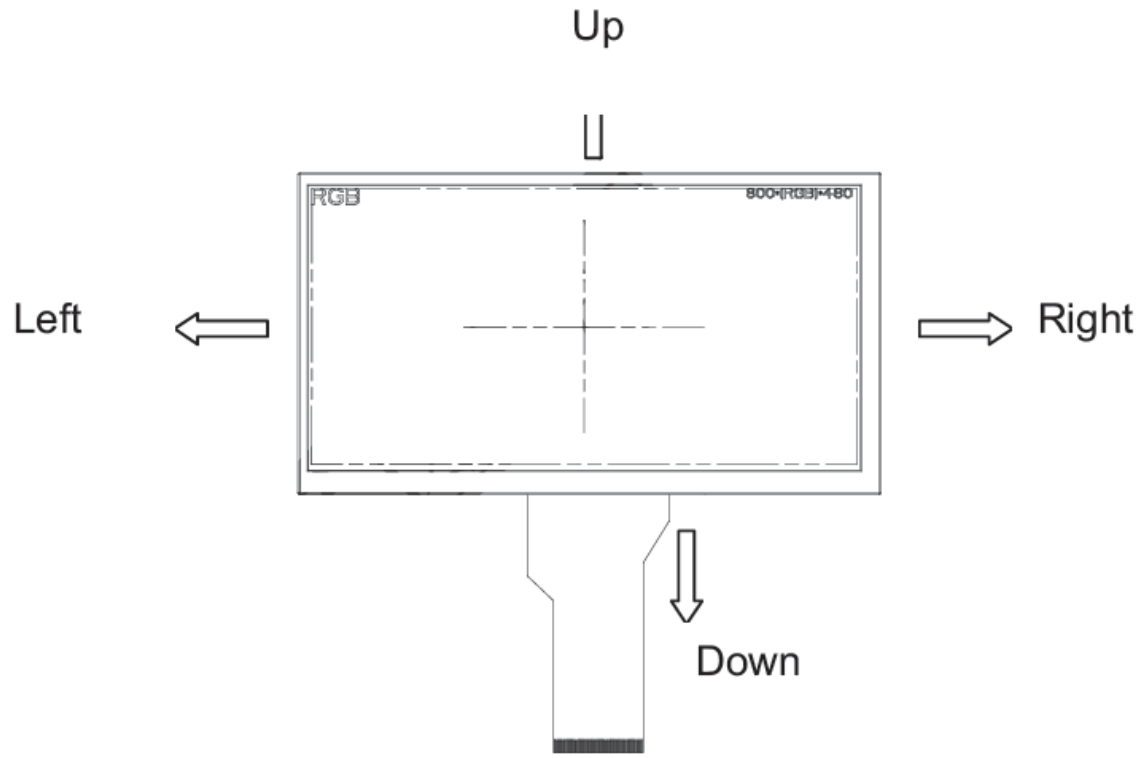
6.3 Interface signals

Pin NO.	Symbol	Description
1	VCOM	Common voltage
2~3	VDD	Digital Power
4	NC	No connection
5	Reset	Global reset pin. Active Low to enter Reset State. Normally pull high. It’s necessary to connecting with an RC delay circuit for stability. (GRB delay VDD larger than 1ms)
6	STBYB	Standby mode, normally pull high STBYB=”1”, Normal Operation STBYB=”0”,Timing control, source driver will turn off, all output are high-Z
7	GND	Ground level for analog block.
8	NIND0	Negative LVDS Differential Data Inputs
9	PIND0	Positive LVDS Differential Data Inputs
10	GND	Ground
11	NIND1	Negative LVDS Differential Data Inputs
12	PIND1	Positive LVDS Differential Data Inputs
13	GND	Ground
14	NIND2	Negative LVDS Differential Data Inputs
15	PIND2	Positive LVDS Differential Data Inputs
16	GND	Ground
17	NINC	Negative LVDS Differential Clock Inputs
18	PINC	Positive LVDS Differential Clock Inputs
19	GND	Ground
20	NIND3	Negative LVDS Differential Data Inputs
21	PIND3	Positive LVDS Differential Data Inputs
22	GND	Ground
23~24	NC	No connection
25	GND	Ground
26~27	NC	No connection
28	SELB	6 bit/8 bit mode select
29	AVDD	Power for Analog Circuit
30	GND	Ground
31~32	LED-	LED Cathode
33	SHLR	Horizontal Inversion
34	UPDN	Vertical Inversion
35	VGL	Negative Power for TFT.
36~37	NC	No connection
38	VGH	Positive Power for TFT.
39~40	LED+	LED Anode

Note 4: Selection of scanning mode

Setting of scan control input		Scanning direction
U/D	L/R	
GND	DV_{DD}	Up to down, left to right
DV_{DD}	GND	Down to up, right to left
GND	GND	Up to down, right to left
DV_{DD}	DV_{DD}	Down to up, left to right

Note 5: Definition of scanning direction.
Refer to the figure as below:



Note 6: Global reset pin. Active low to enter reset state. Suggest to connect with an RC reset circuit for stability. Normally pull high.

Note 7:Dithering function enable control. Normally pull low
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function

Note 8: Reserve for LED power input.

6.OpticalCharacteristics

Item	Symbol		**Condition**	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	-	1000	-	Cd/m^2	1
Uniformity	⊿Bp			75	80	-	%	1,2
Viewing Angle	3:00		Cr≥10	80	85	-	Deg	3
	6:00			80	85	-		
	9:00			80	85	-		
	12:00			80	85	-		
Contrast Ratio	Cr		θ=0° Φ=0°	500	800		-	4
Response Time	T_r+T_f				25	40	ms	5
Color of CIE Coordinate	W	x	θ=0° Φ=0°	TYP -0.05	0.303	TYP +0.05	-	1,6
		y			0.333		-	
	R	x			-		-	
		y			-		-	
	G	x			-		-	
		y			-		-	
	B	x			-		-	
		y					-	

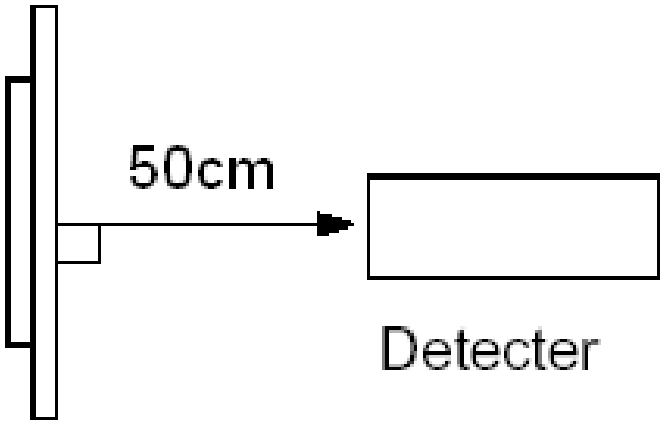
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

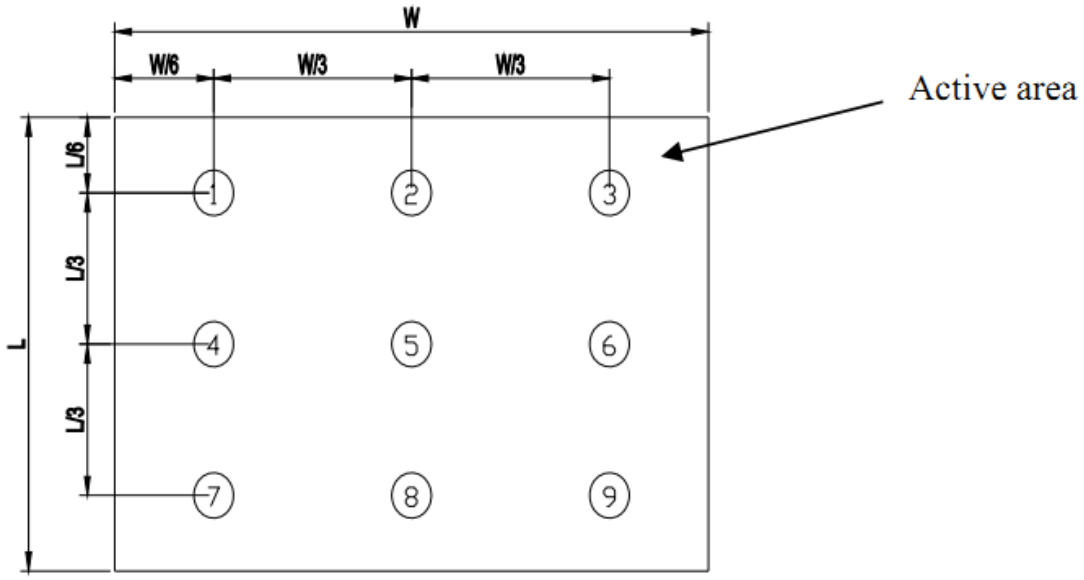


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

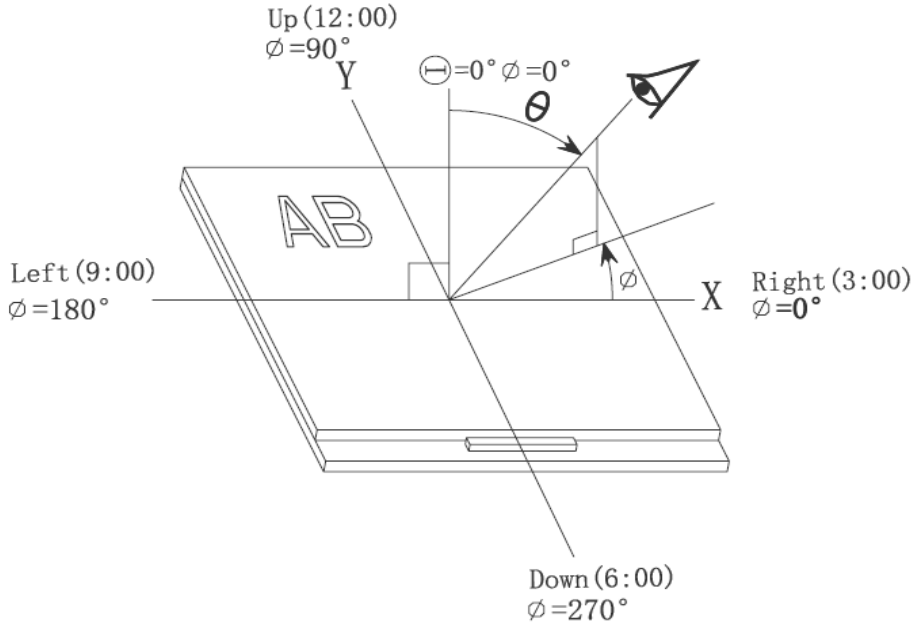
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

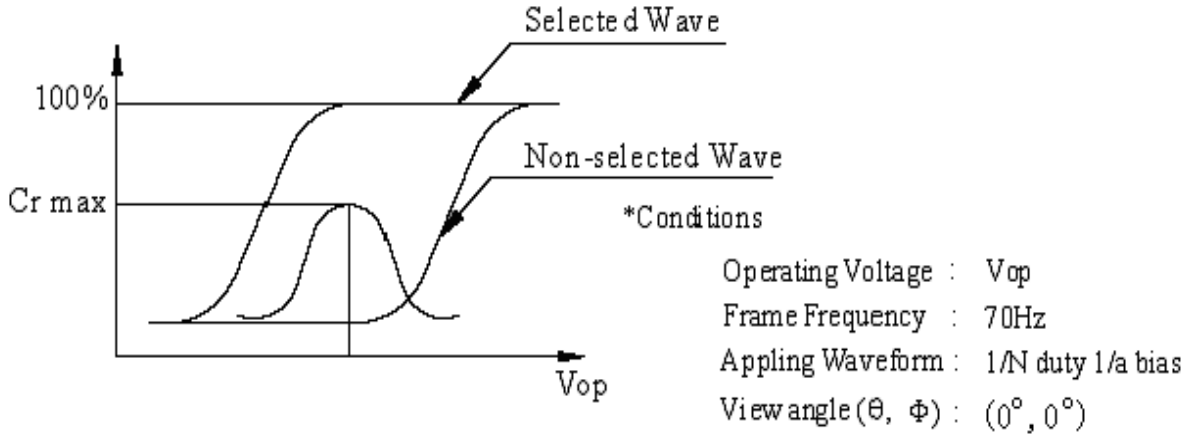


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



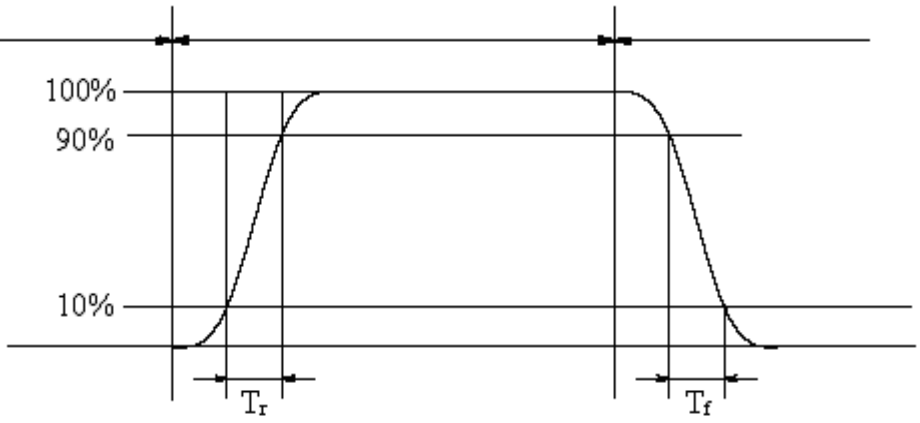
Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

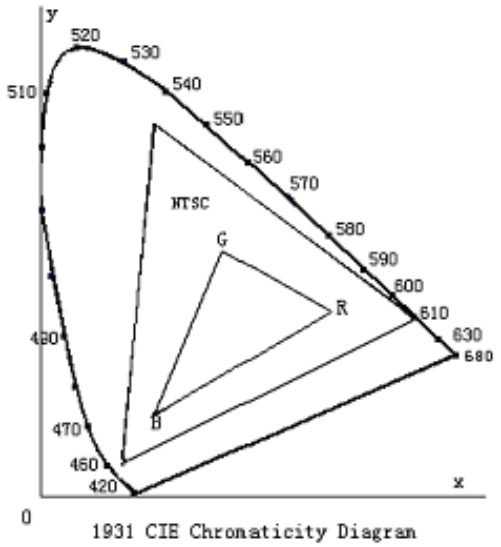
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

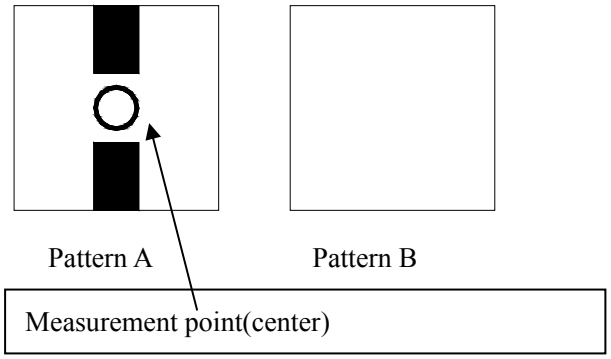


Color gamut:

$$\mathbf{S = \frac{area\ of\ RGB\ triangle}{area\ of\ NTSC\ triangle} \times 100\%}$$

Note 7: Definition of cross talk.

Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100



Electric volume value=3F+/-3Hex

7. Parallel LVDS input timing table

7.1 Resolution: 1024x600

DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1114	1344	1400	DCLK
HSD blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		T_H
VSD period	tv	610	635	800	T_H
VSD blanking	tvbp+tvfp	10	35	200	T_H

Table 10.4: DE mode (1024x600)

HV mode

- **Horizontal timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	44.9	51.2	63	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1200	1344	1400	DCLK
HSD pulse Width	thpw	1	-	140	DCLK
HSD back porch	thbp		160		DCLK
HSD front porch	thfp	16	160	216	DCLK

Table 10.5: HV mode horizontal timing (1024x600)

- **Vertical timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		T_H
VSD period	tv	624	635	750	T_H
VSD pulse width	tvpw	1	-	20	T_H
VSD back porch	tvbp		23		T_H
VSD front porch	tvfp	1	12	127	T_H

Table 10.6: HV mode vertical timing (1024x600)

7.2 LVDS mode data input format

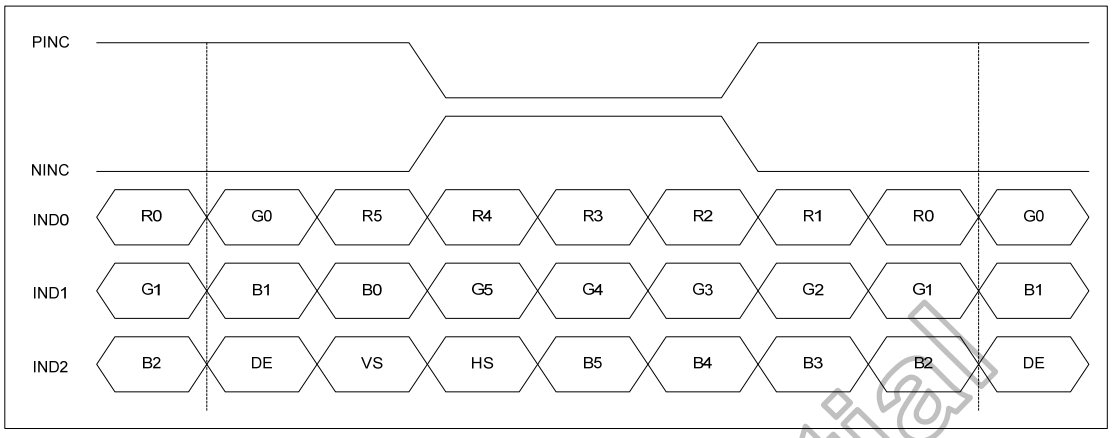


Figure 10.4: 6-bit LVDS input

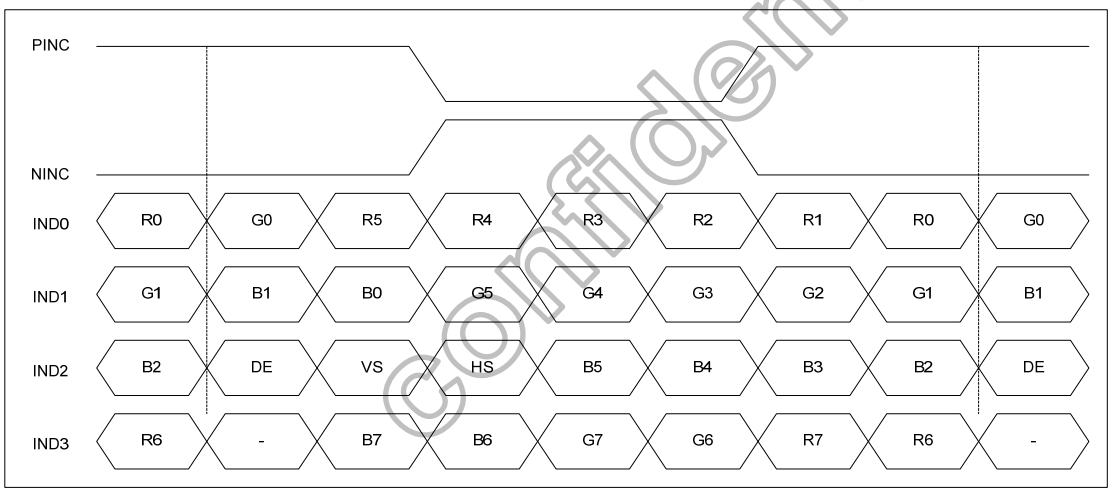


Figure 10.5: 8-bit LVDS input

7.3 PWM power table

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Base drive current for PWM	IDRV	DRVA=0.7V	-	-	60	mA
DRV output voltage for PWM	VDRV	-	0	-	VDD	V
Feed back voltage for PWM	VFB	-	1.15	1.2	1.25	V
Duty cycle maximum	Dmax	-	-	-	76.5	%
VCOM buffer input voltage	VCOMI	-	1	-	AVDD	V
VCOM buffer output voltage	VCOMO	-	VCOMI-0.2	VCOMI	VCOMI+0.2	V
VCOM buffer output current	IVCOM	Fclk=65MHz, VDD=3.3V	-	-	10	mA

Table 9.4: Power table

8. LVDS mode AC electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock frequency	R_{XFCLK}	-	20	-	71	MHz
Input data skew margin	T_{RSKM}	$\| V_{ID} \|$=400mV R_{XVCM}=1.2V R_{XFCLK}=71MHz	500	-	-	pS
Clock high time	T_{LVCH}	-	-	$4/(7xR_{XFCLK})$	-	ns
Clock low time	T_{LVCL}	-	-	$3/(7xR_{XFCLK})$	-	ns
PLL wake-up time	T_{enPLL}	-	-	-	150	μs

Table 10.2: LVDS mode AC electrical characteristics

9. DC Characteristics

9.1 Absolute maximum rating (GND=AGND=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.5	-	+3.96	V
Power supply voltage 2	AVDD	-0.5	-	+14.85	V
Logic output voltage	V_{OUT}	-0.5	-	+5.0	V
Input voltage	V_{IN}	-0.5	-	AVDD+0.5	V
Operation temperature	T_{OPR}	-20	-	+85	℃
Storage temperature	T_{STG}	-55	-	+125	℃

Note: (1) All of the voltages listed above are with respective to GND=0V.
(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

Table 9.1: Absolute maximum rating

9.2 LVDS mode DC electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Differential input high Threshold voltage	R_{XVTH}	R_{XVCM}=1.2V	-	-	+0.1	V
Differential input low threshold voltage	R_{XVTL}		-0.1	-	-	V
Input voltage range **(Singled-end)**	R_{XVIN}	-	0	-	VDD-1.2+ $\|V_{ID}\|/2$	V
Differential input common mode voltage	R_{XVCM}	-	$\|V_{ID}\|/2$	-	VDD-1.2	V
Differential input voltage	$\| V_{ID} \|$	-	0.2	-	0.6	V
Differential input leakage Current	RV_{Xliz}	-	-10	-	+10	μA
LVDS digital operating Current	Iddlvds	Fclk=65MHz, VDD=3.3V	-	15	30	mA
LVDS digital stand-by Current	Istlvds	Clock & all functions are stopped	-	10	50	μA

Table 9.3: LVDS mode DC electrical characteristics

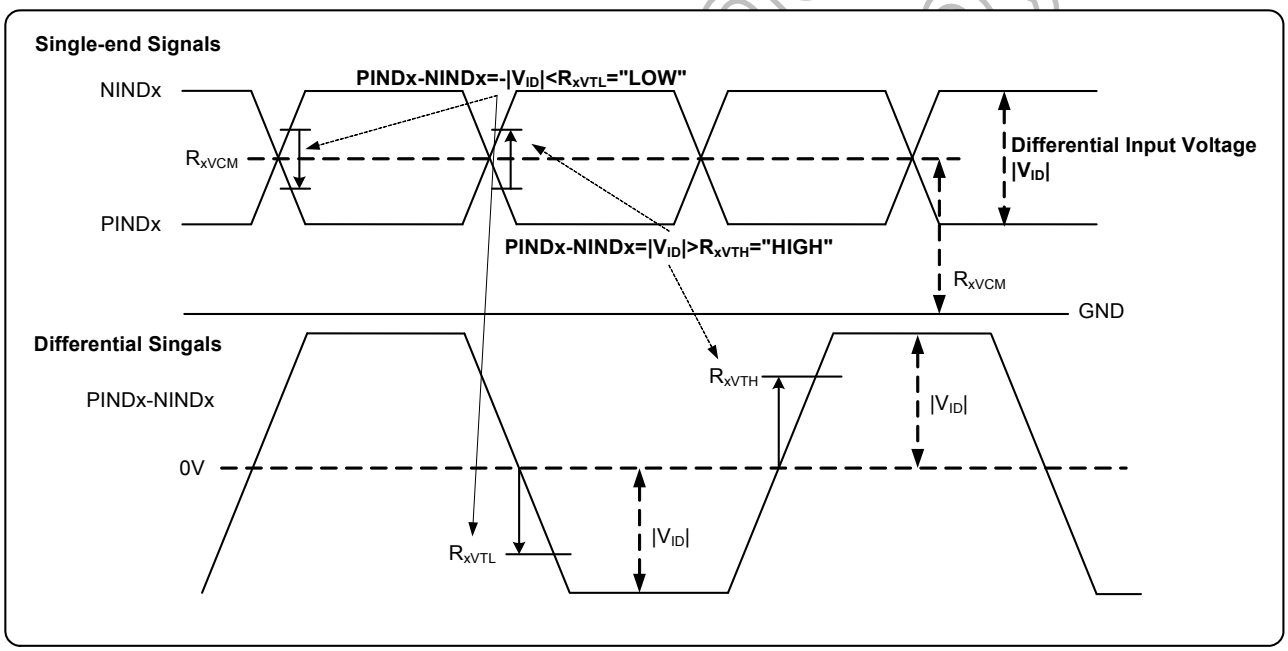


Figure 9.1: Single-end signals

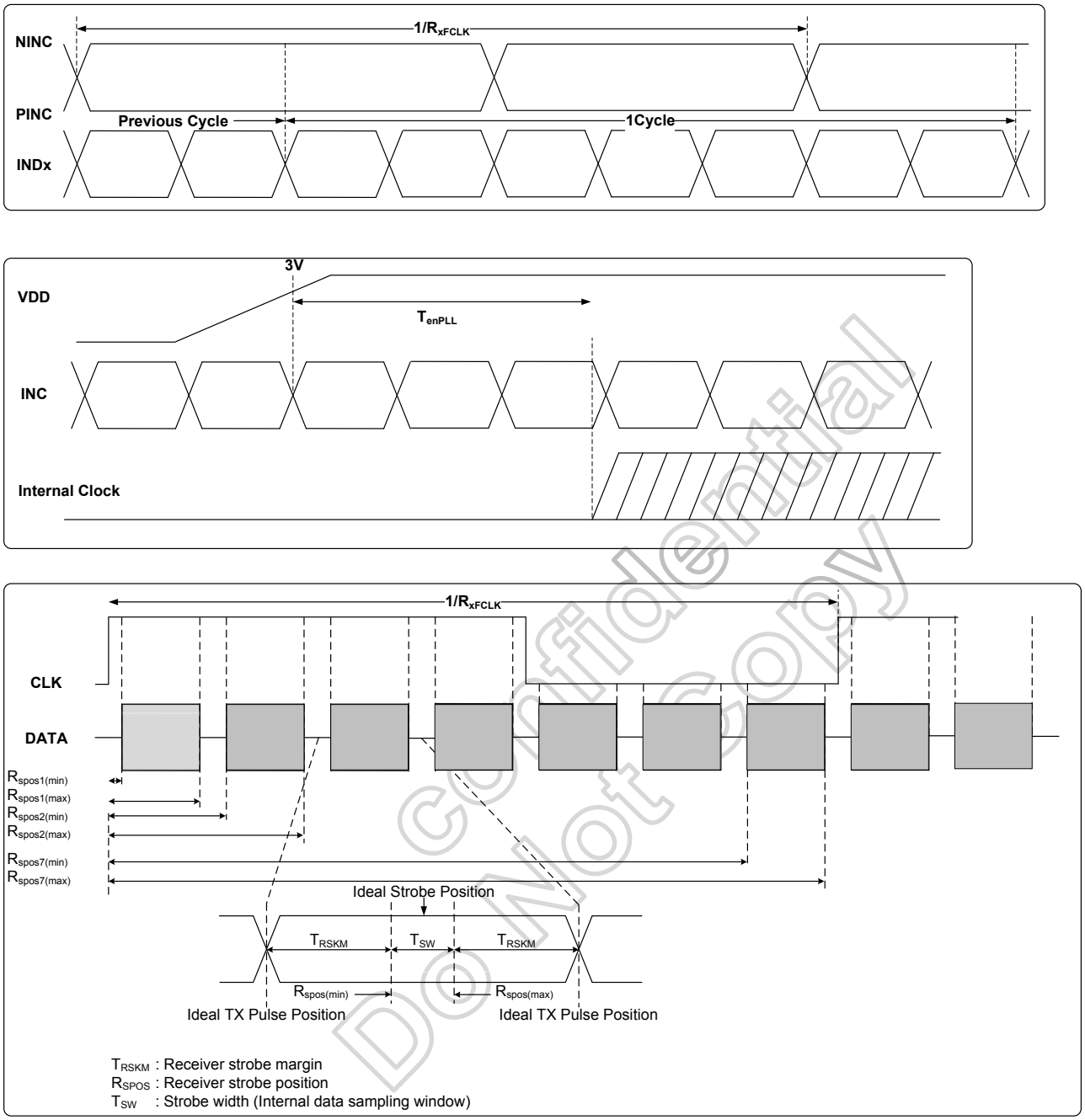


Figure 10.1: LVDS figure

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Modulation frequency	SSC_{MF}	-	23	-	93	KHz
Modulation rate	SSC_{MR}	LVDS clock=71MHz center spread	-	-	±3	%

Table 10.3: SSC table

10. Power On/Off Sequence

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14
Power off: V1 to V14 → AVDD, AGND→ VDD, GND

10.1 Power on/off control

HX8282-A01 has a power on/off sequence control function. In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Please refer to “AC Characteristics” for more detail on timing.

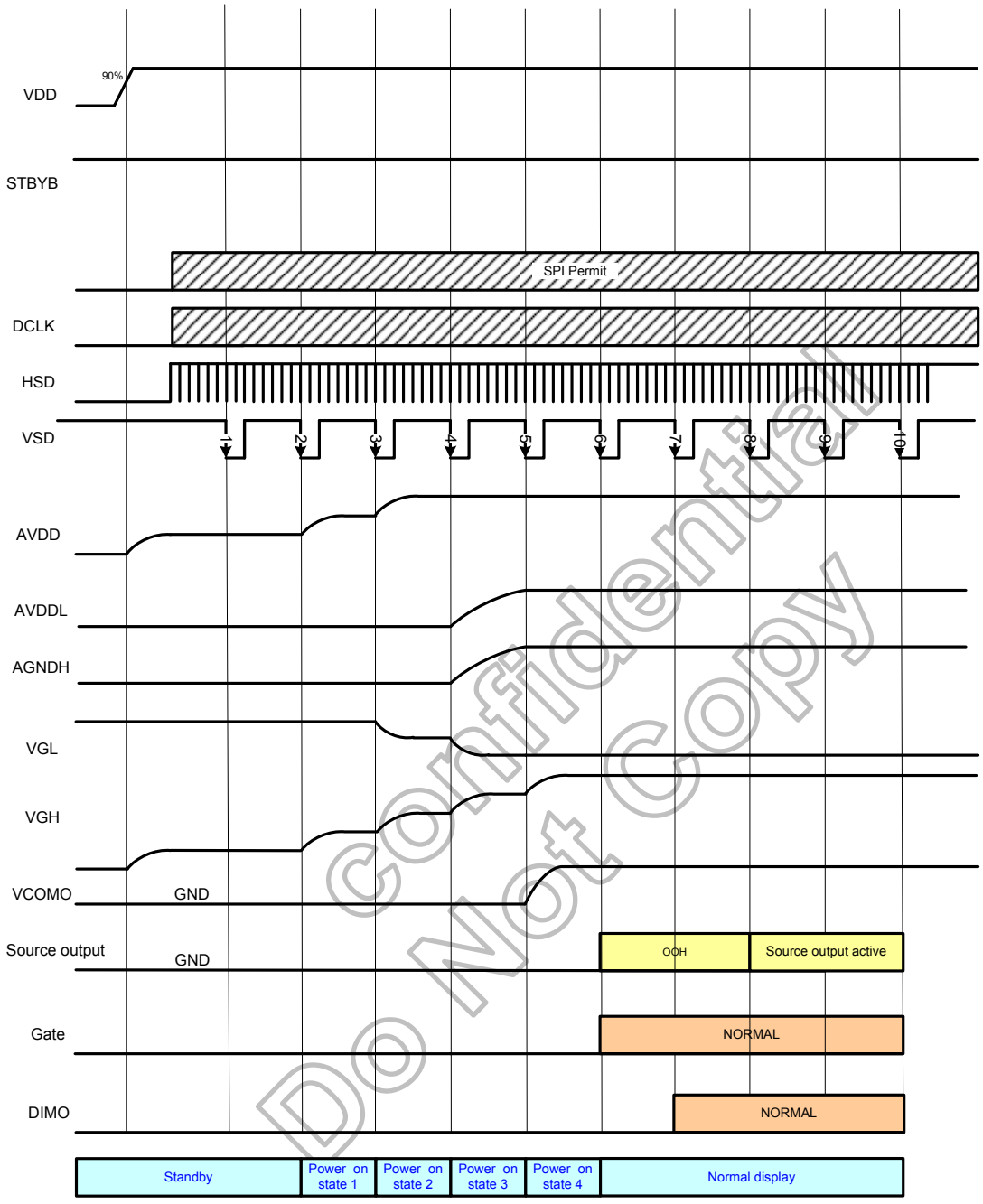
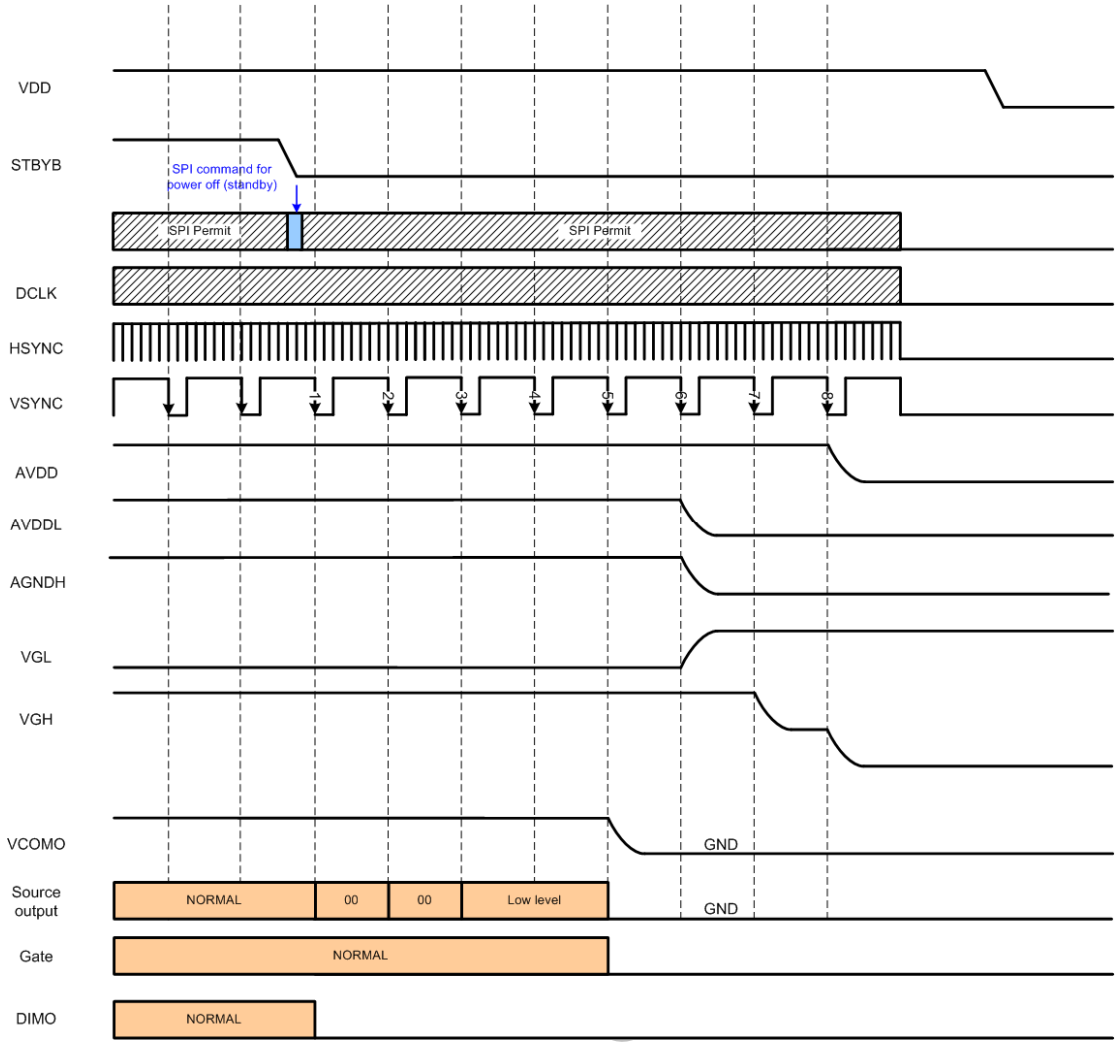


Figure 8.1: Power on timing sequence



Note: (1) Low level=3FH, when NBW=L. **(Normally white)**
(2) Low level=00H, when NBW=H. **(Normally black)**

Figure 8.2: Power off timing sequence

11.ReliabilityTestItemsandCriteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80℃±2℃ 96H Restore 2H at 25℃ Power off	1. After testing, cosmetic and electrical defects should not happen. 2. Total current consumption should not be more than twice of initial value.
2	Low Temperature Storage	-30℃±2℃ 96H Restore 2H at 25℃ Power off	
3	High Temperature Operation	70℃±2℃ 96H Restore 2H at 25℃ Power on	
4	Low Temperature Operation	-20℃±2℃ 96H Restore 4H at 25℃ Power on	
5	High Temperature/Humidity Operation	50℃±2℃ 90%RH 96H Power on	
6	Temperature Cycle(Storage)	–20℃←-25℃-------→70℃ 30min 5min 30min after 5 cycle, Restore 2H at 25℃ Power off	
7	Vibration Test	10Hz~150Hz, 100m/s^2, 120min	Not allowed cosmetic and electrical defects.
8	Shock Test	Half- sine wave,300m/s^2,11ms	
9	ESD Test	Air discharge:+/-8KV, Contact discharge:4KV	

Note: Operation: Supply 3.3V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

12.Qualitylevel

12.1Classificationofdefects

Major defects (MA): A major defect refers to a defect that may substantially

degrade usability for product applications, including all functional defects(such as no display, abnormal display, open or missing segment, short circuit, missing component), outline dimension beyond the drawing, progressive defects and those affecting reliability.

Minor defects (MI): A minor defect refers to a defect which is not considered to be able to substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation, such as black spot, white spot, bright spot, pinhole, black line, white line, contrast variation, glass defect, polarizer defect, etc.

12.2Definitionofinspectionrange

For dot defect of TFT LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area : center of viewing area

B area : periphery of viewing area

C area : Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area

B zone : Outside Viewing area

X1(A.A~V.A): 2mm X2(A.A~V.A): 2mm

Y1(A.A~V.A): 2mm Y2(A.A~V.A): 2mm

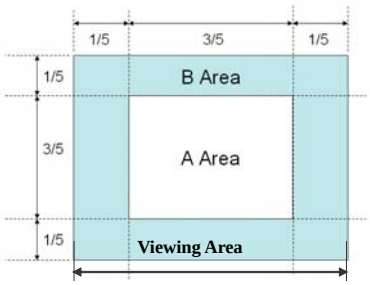


Figure 1

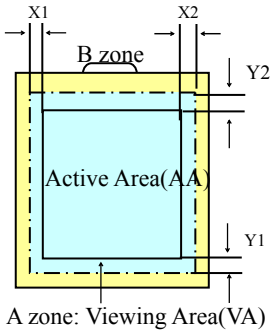


Figure 2

12.3Inspectionitemsandgeneralnotes

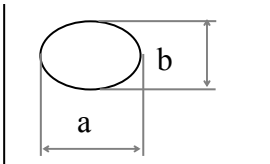
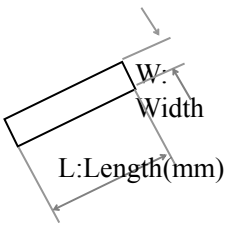
General notes	1.Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and SH. 2.Viewing area should be the area which SH guarantees. 3.Limit sample should be prior to this Inspection standard. 4.Viewing judgment should be under static pattern. 5.Inspection conditions Inspection distance: 250 mm (from the sample) Temperature : 25±5 ºC Inspection angle : 45 degrees in 6 o'clock direction (all defects in viewing area should be inspected from this direction)	
Inspection items	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon doesn't change with voltage
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage
	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass
	Dot defect (TFT LCD)	The pixel appears bright or dark abnormally when display
	Functional defect	No display, Abnormal display, Open or missing segment, Short circuit, False viewing direction

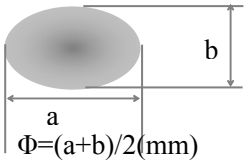
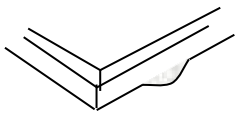
	Glass defect	Glass crack, Shaved corner of glass, Surplus glass
	PCB defect	Components assembly defect

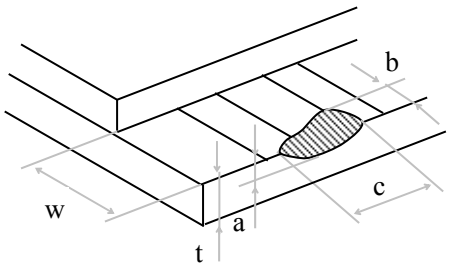
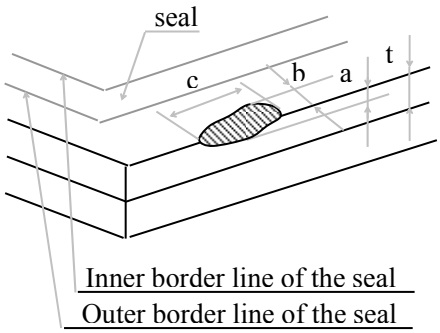
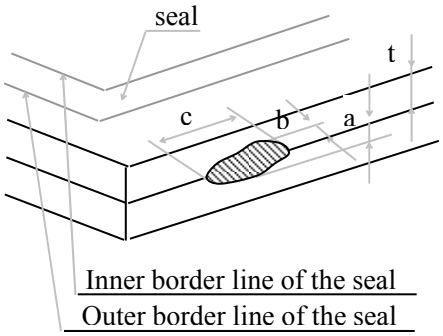
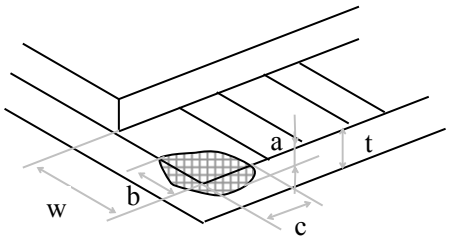
12.4OutgoingInspectionlevel

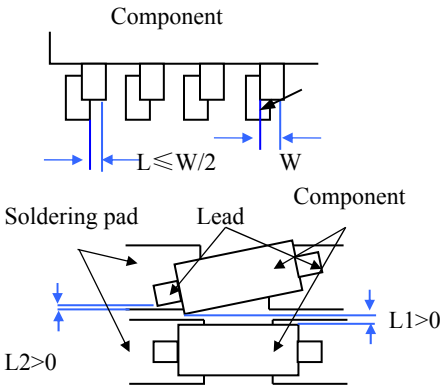
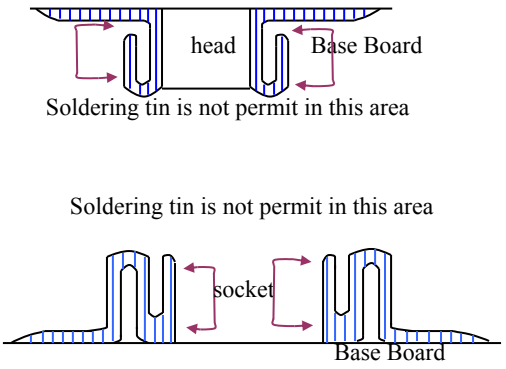
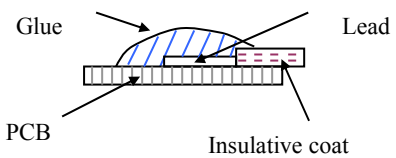
Outgoing Inspection standard	Inspection conditions	Inspection				
		Min.	Max.	Unit	IL	AQL
Major Defects	See 8.3 general notes	See 8.5			II	0.065
Minor Defects	See 8.3 general notes	See 8.5			II	0.065
Note：Sampling standard conforms to GB2828						

12.5InspectionItemsandCriteria

Inspection items			Judgment standard			
			Category		Acceptable number	
					A zone	B zone
1	Black spot, White spot, Pinhole, Foreign Particle, Particle in or on glass, Scratch on glass	 (a/b<2.5)	A	Φ<=0.20	Neglected	Neglected
			B	0.20<Φ<=0.25	3	Neglected
			C	0.25<Φ<=0.3	2	Neglected
			D	0.3<Φ<=0.4	1	3
			E	0.4<Φ<=0.5	0	2
			Total defective point(B,C)		1	-
2	Black line, White line, and Particle Between Polarizer and glass, Scratch on glass	 L/W>=2.5	A	W<=0.03	Neglected	Neglected
			B	0.03<W<=0.05 L<=3.0	3	Neglected
			C	0.05<W<=0.1 L<=3.0	2	Neglected
			D	0.05<W<=0.1 L<=4.0	1	3
			E	W>0.1 L>4.0	0	2
			Total defective point(B,C)		1	-

<table>
<tr><td>3</td><td colspan="2">Bright spot</td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
<tr><td rowspan="5">4</td><td rowspan="5">Contrast variation</td><td rowspan="5"> 
</td><td>A</td><td>Φ<0.2</td><td>Neglected</td><td rowspan="4">Neglected</td></tr>
<tr><td>B</td><td>0.2<Φ<=0.3</td><td>2</td></tr>
<tr><td>C</td><td>0.3<Φ<=0.4</td><td>1</td></tr>
<tr><td>D</td><td>0.4<Φ</td><td>0</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td><td>3</td><td></td></tr>
<tr><td>5</td><td colspan="2">Bubble inside cell</td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">Polarizer defect (if Polarizer is used)</td><td>Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass.</td><td colspan="4">Refer to item 1 and item 2.</td></tr>
<tr><td rowspan="3">Bubble, dent and convex</td><td>A</td><td>Φ<=0.1</td><td>Neglected</td><td>Neglected</td></tr>
<tr><td>B</td><td>0.1 <Φ<=0.2</td><td>2</td><td>Neglected</td></tr>
<tr><td>C</td><td>0.2 <Φ<=0.3</td><td>1</td><td>2</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">Surplus glass</td><td>Stage surplus glass
 
</td><td colspan="4">B<=0.3mm</td></tr>
<tr><td>Surrounding surplus glass
  </td><td colspan="4">Should not influence outline dimension and assembling.</td></tr>
<tr><td>8</td><td colspan="2">Open segment or open common</td><td colspan="4">Not permitted</td></tr>
<tr><td>9</td><td colspan="2">Short circuit</td><td colspan="4">Not permitted</td></tr>
<tr><td>10</td><td colspan="2">False viewing direction</td><td colspan="4">Not permitted</td></tr>
<tr><td>11</td><td colspan="2">Contrast ratio uneven</td><td colspan="4">According to the limit specimen</td></tr>
<tr><td>12</td><td colspan="2">Crosstalk</td><td colspan="4">According to the limit specimen</td></tr>
<tr><td>13</td><td colspan="2">Black /White spot(display)</td><td colspan="4">Refer to item 1</td></tr>
<tr><td>14</td><td colspan="2">Black /White line(display)</td><td colspan="4">Refer to item 2</td></tr>
</table>

<table>
<tr><th colspan="3" rowspan="2">Inspection items</th><th colspan="2">Judgment standard</th></tr>
<tr><th colspan="2">Category(application: B zone)</th><th>Acceptable number</th></tr>
<tr><td rowspan="5">15</td><td rowspan="5">Glass defect crack</td><td>i) The front of lead terminals
 
</td><td>A</td><td>a≤ t, b≤1/5W, c≤3mm</td><td rowspan="5">Max.3 defects allowed</td></tr>
<tr><td>B</td><td>Crack at two sides of lead terminals should not cover patterns and alignment mark</td></tr>
<tr><td>ii) Surrounding crack–non-contact side
 
</td><td colspan="2">b < Inner borderline of the seal</td></tr>
<tr><td>iii) Surrounding crack– contact side
 
</td><td colspan="2">b < Outer borderline of the seal</td></tr>
<tr><td>iv) Corner
 
</td><td>A</td><td>a <= t, b <= 3.0, c <= 3.0</td></tr>
<tr><td>B</td><td>Glass crack should not cover patterns u and alignment mark and patterns.</td></tr>
</table>

Inspection items			Judgment standard Category(application: B zone)
16	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1)； the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	
		lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	
		Glue on root of the speaker receiver and motor lead: The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	

13. Precautions for Use of LCD Modules

13.1 Handling Precautions

13.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

13.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

13.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

13.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

13.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

13.1.6 Do not attempt to disassemble the LCD Module.

13.1.7 If the logic circuit power is off,do not apply the inputs ignals.

13.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct

assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13.2 Storage precautions

13.2.1 When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

13.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3TheLCDmodulesshouldbestor ed in the room without acid, alkali and harmful gas.

13.3 The LCD modules should be no falling and violent shockin gduring transportation, and also should avoid excessive press, water, damp and sunshine.